

Appl. No. 10/734,905
Amdt. dated June 2, 2006
Reply to Office Action of December 2, 2005

PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

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PATENT

1 2. (Previously Presented) The method of claim 1 wherein the design criteria
2 includes optimizing for area.

1 3. (Previously Presented) The method of claim 1 wherein the design criteria
2 includes optimizing for delay.

1 4. (Previously Presented) The method of claim 1 wherein the first mapping
2 netlist comprises look-up table structures.

1 5. (Cancelled).

1 6. (Previously Presented) The method of claim 1 wherein the first alternative
2 netlist comprises logic gates.

1 7. (Previously Presented) The method of claim 1 wherein the step of
2 performing a technology mapping of the first alternative netlist to obtain a first mapping netlist is
3 done on a copy of the first alternative netlist.

1 8. (Currently Amended) A method of logic synthesis comprising:
2 generating a first alternative netlist for a logic function;
3 generating a second alternative netlist for the logic function, wherein the second
4 alternative netlist has a different gate configuration from the first alternative netlist; and
5 selecting one of the first alternative netlist or the second alternative netlists as a
6 selected alternative netlist based on results of a technology mapping of the first alternative netlist
7 and the second alternative netlists, ~~wherein the first alternative netlist includes a digital signal~~
8 ~~processing block;~~ and
9 optimizing the selected netlist based on results of a technology mapping of the
10 first alternative netlist and the second alternative netlists; and
11 performing a technology mapping on the selected mapping netlist after
12 optimizing.

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PATENT

1 9. (Previously Presented) The method of claim 8 further comprising:
2 performing a synthesis optimization on the selected alternative netlist to obtain an
3 optimized selected alternative netlist.

1 10. (Previously Presented) The method of claim 8 further comprising:
2 performing a synthesis optimization on the selected alternative netlist to obtain an
3 optimized selected alternative netlist; and
4 performing a technology mapping on the optimized selected alternative netlist.

1 11. (Previously Presented) The method of claim 8 wherein the selecting one of
2 the first alternative netlist or the second alternative netlists is based on area.

1 12. (Previously Presented) The method of claim 8 wherein the selecting one of
2 the first alternative netlist or the second alternative netlists is based on depth.

1 13. (Currently Amended) A method of logic synthesis comprising:
2 generating a netlist for a logic function;
3 performing a first technology mapping on the netlist;
4 after the first technology mapping, performing a synthesis optimization on the
5 netlist; and
6 after the synthesis optimization, performing a second technology mapping on the
7 netlist, ~~wherein the first technology mapping includes a digital signal processing block.~~

1 14. (Previously Presented) The method of claim 13 wherein the first
2 technology mapping maps the netlist to the same target technology as the second technology
3 mapping.

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1 15. (Previously Presented) The method of claim 13 wherein the logic function
2 is provided in a high-level design language.

1 16. (New) The method of claim 1 wherein the first mapping netlist comprises
2 digital signal processing blocks.

1 17. (New) The method of claim 8 wherein the first alternative netlist
2 comprises digital signal processing blocks.

1 18. (New) The method of claim 13 wherein the first technology mapping
2 comprises digital signal processing blocks.

1 19. (New) The method of claim 1, wherein performing the technology
2 mappings of the first and second alternative netlists comprises estimating technology mappings
3 of the first and second alternative netlists to obtain the first and second mapping netlists.

1 20. (New) The method of claim 13, wherein performing the synthesis
2 optimization on the netlist includes optimizing the netlist based on the results of the first
3 technology mapping.